

What Is Claimed Is:

1 1. A reset pulse generator for a CPU, which generating
2 an oscillating disable signal after initialization, comprising:
3 an oscillating circuit coupled to the CPU to output a
4 sequence of reset pulses to the CPU; and
5 an oscillating disable circuit coupled to the oscillating
6 circuit for disabling the oscillating circuit and
7 initiating normal mode CPU operation when the
8 oscillating disable signal is received.

1 2. The reset pulse generator as claimed in claim 1,
2 wherein the oscillating circuit comprises:
3 a Schmitt trigger having an input terminal and an output
4 terminal;
5 a resistor coupled between the input terminal and the
6 output terminal; and
7 a capacitor coupled to the input terminal and a ground
8 level.

1 3. The reset pulse generator as claimed in claim 1,
2 wherein the oscillating disable circuit is a switch turned on
3 by the oscillating disable signal to stop oscillation of the
4 oscillating circuit.

1 4. The reset pulse generator as claimed in claim 1,
2 further comprising a manual switch to generate a start signal
3 to enable the oscillating circuit.

1 5. The reset pulse generator as claimed in claim 1,
2 wherein the start signal is generated during power on.

1 6. A reset pulse generator, comprising:
2 a CPU for generating an oscillating disable signal after
3 initialization;
4 an oscillating circuit coupled to the CPU to output a
5 sequence of reset pulses to the CPU; and
6 an oscillating disable circuit coupled to the oscillating
7 circuit for disabling the oscillating circuit and
8 initiating normal mode CPU operation when the
9 oscillating disable signal is received.

1 7. The reset pulse generator as claimed in claim 6,
2 wherein the oscillating circuit comprises:
3 a Schmitt trigger having an input terminal and an output
4 terminal;
5 a resistor coupled between the input terminal and the
6 output terminal; and
7 a capacitor coupled to the input terminal and a ground
8 level.

1 8. The reset pulse generator as claimed in claim 6,
2 wherein the oscillating disable circuit is a switch turned on
3 by the oscillating disable signal to stop oscillation of the
4 oscillating circuit.

1 9. The reset pulse generator as claimed in claim 6,
2 further comprising a manual switch to generate a start signal
3 to enable the oscillating circuit.

1 10. The reset pulse generator as claimed in claim 6,
2 wherein the start signal is generated during power on.